EXPERIMENT 5

MAGNITUDE COMPARATOR

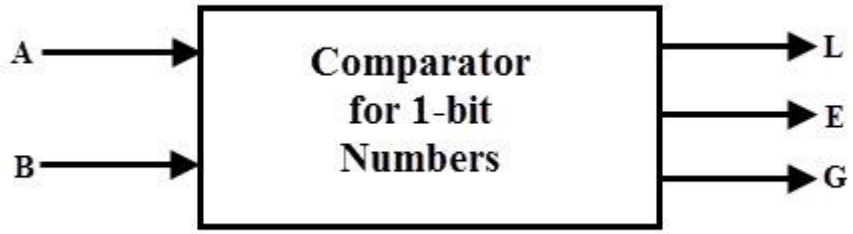
THEORY

Comparators with three output terminals and checks for three conditions i.e greater than or less than or equal to is magnitude comparator.

Single Bit Magnitude Comparator

A comparator used to compare two bits, i.e., two numbers each of single bit is called a single bit comparator. It consists of two inputs for allowing two single bit numbers and three outputs to generate less than, equal and greater than comparison outputs.

The figure below shows the block diagram of a single bit magnitude comparator. This comparator compares the two bits and produces one of the 3 outputs as L (A<B), E (A=B) and G (A>B).



The truth table for the single bit comparator is given below. When A0 B0 = 00 & 11, both inputs are equal, therefore A=B output will be high. When A0 B0 = 01, B is more than A and hence AB is active.

A_0	B_0	L	E	G
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

EXPERIMENTAL PROCEDURE

1) Design a ***single bit magnitude comparator*** by using logic gates.

Equipment List:

1) 74LS32 TTL ***OR*** GATE IC
2) 74LS08 TTL ***AND*** GATE IC
3) 74LS04 TTL ***NOT*** GATE IC
4) Standard set equipments