EXPERIMENT 4

COMBINATIONAL LOGIC CIRCUITS AND ADDERS

OBJEJTIVE
To gain experience in logic circuits and Adders.

HALF ADDER

A half adder is a digital logic circuit with two input terminals and two output terminals. The output terminals are called the sum and carry outputs. The sum output of a half-adder circuit is the ***exclusive OR*** (***XOR***) function of the two inputs. That is, the sum output is 0 when the inputs are the same and 1 when they are different. The carry output is the ***AND*** function of the two inputs. It is 1 only when both inputs are 1.

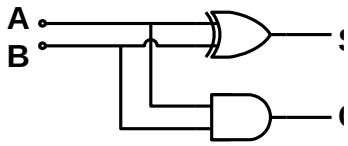
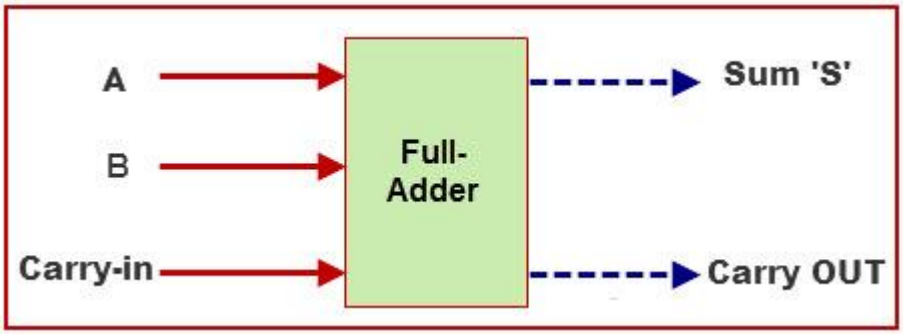


Figure 4.1. Implementation of a half-adder.

FULL ADDER

This adder is difficult to implement than a half-adder. The difference between a half-adder and a full-adder is that the full-adder has three inputs and two outputs, whereas half adder has only two inputs and two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. When a full-adder logic is designed, you string eight of them together to create a byte-wide adder and cascade the carry bit from one adder to the next.



The output carry is designated as C-OUT and the normal output is designated as S.

FULL ADDER TRUTH TABLE

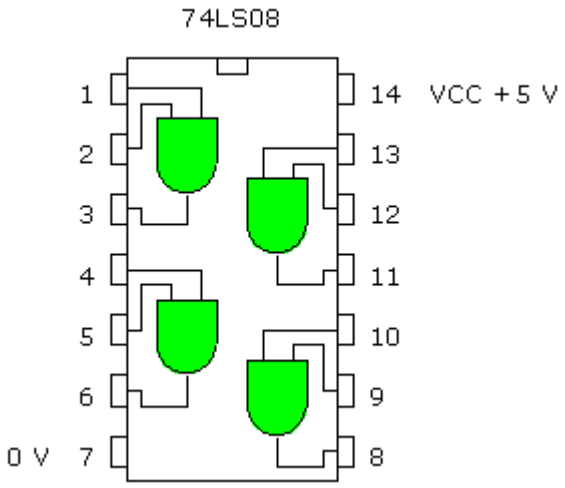
INPUTS			OUTPUT	
A	B	C-IN	C-OUT	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

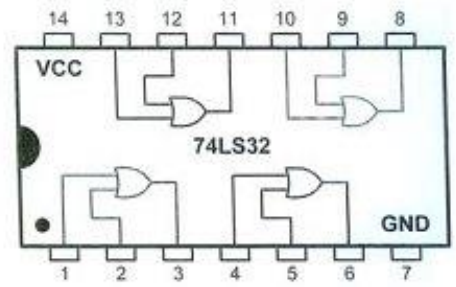
EXPERIMENTAL PROCEDURE

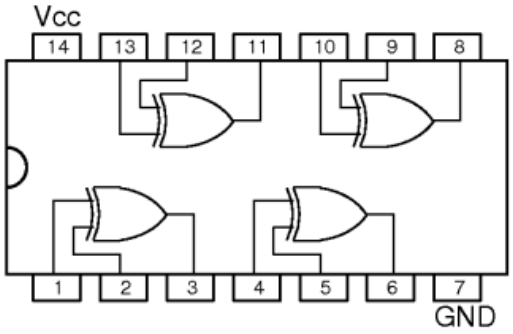
1) Implement full adder by using minimum amount of logic gates.

Equipment List

1) 74LS32 TTL ***OR*** GATE IC
2) 74LS08 TTL ***AND*** GATE IC
3) 74LS86 TTL ***XOR*** GATE IC
4) Standard set equipments







7486 Quad 2 Input XOR