EXPERIMENT 2

COMBINATIONAL LOGIC CIRCUITS AND KARNOUGH MAP

OBJEJTIVE
To gain experience in using logic circuits and Karnough map

THEORY

Simplification of logic circuits is a responsibility of the designer. Simpler circuits are generally more economic and more reliable.

SUM OF PRODUCT FORM (SOP)

The sum of product form of a logic circuit output looks like the following examples:

$$F(A,B,D) = A\overline{B}D + A\overline{B}\,\overline{D}$$
$$F(A,B,C,D,E,F,H) = \overline{A}B + C\overline{D} + EF + \overline{H}F$$

Logic equations may also be simplified using Boolean algebra or Karnough map. Both types of simplification will be covered the logic equations shown in the above examples are called “minterm” expressions.

Minterm expressions are logical equations where logical sum operator separates the logical product terms. Minterm expressions are also called sum of product expressions.

DESIGNING COMBINATIONAL CIRCUIT

Logic design begins with a problem statement. The problem statement is analyzed and translated into logic variable inputs. A truth table is then constructed to show when a logic one output is to be produced. Next a SOP (minterm) logic equation is then produced. Then a circuit is drawn from the SOP logic equation.

THE KARNOUGH MAP

A Karnough map or K-map technique is a graphical device to simplify logic equations or the output of truth tables following a simple orderly process.

A K-map like a truth table displays the relationship between input variables and the desired or true output of logic expression on the truth table.

EXAMPLE: Simplify the logical equation by using K-map $F(A,B,C) = \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + A\overline{B}\overline{C} + AB\overline{C}$

Truth Table			
A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Table 3.1 Truth table of logical function

AB / C	00	01	11	10
0	1	0	1	1
1	1	0	0	0

Fig 3.1 K-map of the function

After using K-map Simplified logical expression is $F = A\overline{C} + \overline{A}\overline{B}$

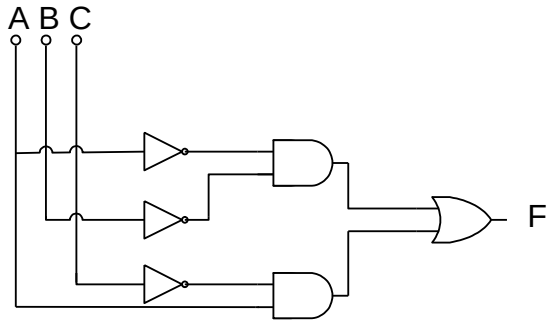

Fig 3.2 Logic Circuit

EXPERIMENTAL PROCEDURE

1) f(a,b,c)=∑(0,1,5,6,7)
2) Simplify the logical expression of the problem by using K-map
3) Implement simplified logical expression using logic gates.

EQUIPMENT LIST:

1) 74LS32 TTL OR GATE IC
2) 74LS08 TTL AND GATE IC
3) 74LS04 TTL NOT GATE IC
4) Standard set equipments